# The DRE, the digital readout electronics for Athena X-IFU

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#### ABSTRACT

We are developing the digital readout electronics (DRE) of the X-Ray Integral Field Unit (X-IFU), one of the two Athena focal plane instruments. This subsystem is made of two main parts: the DRE-DEMUX and the DRE-EP. With a frequency domain multiplexing (FDM) the DRE-DEMUX makes the readout of the 3840 Transition Edge Sensors (TES) in 96 channels of 40 pixels each. It provides the AC signals to voltage-bias the TES, it demodulates the detector's data which are readout by a SQUID and low noise amplifiers and it linearizes the detection chain to increase its dynamic range. The feedback is computed with a specific technique, so called baseband feedback (BBFB) which ensures that the loop is stable even with long propagation and processing delays (i.e. a few  $\mu$ s) and with high frequency AC-bias (up to 5 MHz). This processing is partly analogue (anti aliasing and reconstruction filters) but mostly digital. The digital firmware is simultaneously applied to all the pixels in digital integrated circuits. After the demultiplexing the interface between the DRE-DEMUX and the DRE-EP has to cope with a data rate of 61.44 Gbps to transmit the data of the individual pixels. Then, the DRE-EP detects the events and computes their energy and grade according to their spectral quality: low resolution, medium resolution and high resolution (i.e. if two consecutive events are too close the estimate of the energy is less accurate). This processing is done in LEON based processor boards. At its output the DRE-EP provides the control unit of the instrument with a list including for each event its time of arrival, its energy, its location on the focal plane and its grade.

Keywords: Readout Electronics, Frequency Domain Multiplexing, Baseband Feedback, Optimal Filtering

# 1. INTRODUCTION

The Advanced Telescope for High Energy Astrophysics (*Athena*) has been proposed to ESA as the second large mission of its Cosmic Vision program. Aiming to address the "hot and energetic Universe" science theme the *Athena* observatory will have an X-ray telescope and two focal plane instruments: The Wide Field Imager (WFI) and the X-ray Integral Field Unit (X-IFU).<sup>1–3</sup> The X-IFU is a high-resolution 3D spectrometer using an array of 3 840 Transition Edge Sensors (TES) cooled at 50 mK to achieve an energy resolution as good as 2.5 eV at 6 keV. With a Frequency Domain Multiplexing (FDM) technique the focal plane array is readout with 96 channels of 40 pixels each. At 50 mK this is implemented with a Cold Front End Electronics (CFEE) which includes i) a matrix of LC filters, each of them being associated with a TES sensor to select a narrow part of the frequency range (i.e. a few kHz) and ii) in each channel, a Superconducting Quantum Interference Device (SQUID) to readout the current of the detectors. Outside the cryostat, after amplification by the Warm Front End Electronics (WFEE), the signal of each channel is processed by the demultiplexer of the Digital Readout Electronics (DRE-DEMUX) to retrieve the data of each pixel. This will be presented in section 2. Afterwards

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the event processor unit (DRE-EP) analyses the data of the pixels to detect and characterize the events. This will be presented in section 3. A block diagram of the X-IFU where the DRE has been highlighted is shown in Fig. 1. The requirements of the X-IFU readout chain are detailed in Ref. 4.



Figure 1. Block diagram of the X-IFU instrument. The digital readout electronics is highlighted with a bold rectangle.

# 2. THE DEMULTIPLEXER UNIT (DRE-DEMUX)

# 2.1 The Frequency Domain Multiplexing (FDM)

To do the FDM readout of the X-IFU focal plane array, the DRE-DEMUX provides an AC-carrier signal to each channel. This analogue signal contains one AC-bias signal per pixel. When an X-ray interacts with a TES and its absorber, the temperature and the resistance of the TES increase. As a consequence the quality factor of the TES resonator decreases and the TES current is amplitude-modulated (see Fig. 2). The sum of the TES currents is read by a SQUID and propagated to the DRE-DEMUX through an amplification chain (SQUID arrays in the cold part and a second stage with low noise amplifiers in the WFEE). To linearize the readout chain (particularly the first stage SQUID) the DRE-DEMUX has to compute and to provide a feedback signal. Because of the propagation time in the long harness through the *Athena* payload module (a few meters) and of the feedback processing time (several  $\mu$ s), a "standard" feedback technique cannot maintain the feedback loop stable in the 1 - 5 MHz frequency range where the AC-biases lie. For the X-IFU we will use the so-called Baseband Feedback (BBFB) technique developed by SRON for the *Safari* instrument onboard SPICA.<sup>5,6</sup>



Figure 2. Principle of the Frequency Domain Multiplexing (FDM). Left) Example of a 3-pixel reception and readout channel: each TES is associated with a LC cell to select a narrow frequency range. Top-right) Transfer function of each branch (dotted lines) and of the full matrix (solid line). An X-ray interacting with TES 1 and its absorber changes the transfer function. Bottom-right) Currents in each branch of the TES and LC circuit. The X-ray amplitude-modulates the current of TES 1. The sum of the currents is read by the SQUID and will be demultiplexed by the DRE-DEMUX.

#### 2.2 The BaseBand FeedBack (BBFB)

The BBFB digital algorithm makes the feedback properly phased with the TES signal at the SQUID input in order to minimize the amplitude of the signal to be processed by the SQUID. To do that, for each TES pixel of the channel, the BBFB firmware frequency-shifts the SQUID output signal with I/Q demodulators in order to place the TES data in the DC. Digital integrators compute the science signal from these "DC data". Finally the science signal of each TES is shifted back to its AC-bias frequency and they are all added together to build the feedback signal. During the I/Q demodulation and remodulation operations a phase correction is applied to compensate for the propagation and processing delays. The phase correction is specific to each pixel, it depends

on the delay that has to be corrected and on the AC-bias frequency. This processing is done in parallel for each pixel of the channel.<sup>5</sup> An X-IFU channel with its BBFB processing is shown in Fig. 3.

To configure a BBFB module so that it can process the data of one pixel, 6 parameters are needed: 1) The AC-carrier amplitude shall be approximately the same for all the TES. In the control electronics it shall then be possible to tune the amplitude per pixel to compensate the frequency dependent attenuation between the warm electronics and the detectors. 2) We have to set each carrier frequency so that it matches its TES and LC resonance frequency, 3) The phase correction shall compensate for the delays in the loop at the carrier frequency, 4) The gain-bandwidth product of the BBFB loop shall be set to ensure the stability of the system. 5) The initial phase of the individual AC-biases shall be adjusted to optimize the dynamic range of the DACs. 6) A carrier rotation with respect to the demodulating signal is needed to compensate for the weak-link behavior of the TES.<sup>7</sup> For the whole focal plane array (i.e. 3840 pixels) we have to optimally set approximately 23000 parameters. It is then mandatory to use an automated procedure in order to characterize the whole system and to automatically define the optimal values for all these parameters.

We have defined such an automated procedure to characterize efficiently the detection chain and to define the set of optimal parameters to be applied to the BBFB firmware.<sup>5</sup> This procedure is regularly used at SRON during the test campaigns of the TES and their front-end FDM readout electronics.



Figure 3. Baseband Feedback technique applied to X-IFU.

#### 2.3 Data rates

In the readout channels the frequencies of the 40-carrier signals used to AC-bias the TES detectors are spread between 1 and 5 MHz with a spacing of 100 kHz. Thanks to very sharp filters (i.e. anti-aliasing filtering before the ADCs and reconstruction filtering after the DACs) the sampling of the data and the processing of the BBFB algorithm in the digital integrated circuits is done at 20 MHz. After the demultiplexing, because the science signal bandwidth is a few hundreds of kHz only, the pixel data are filtered and sampled at 1 MHz. As the data are coded with 16 bits, considering the 3840 pixels of the instrument, this leads to a data rate at the interface between the DRE-DEMUX and the DRE-EP of 61.44 Gbps. This data rate does not depend on the observed source count rate.

# 3. THE EVENT PROCESSOR UNIT (DRE-EP)

After being pre-processed by the DRE-DEMUX the digital data stream is analyzed by the Event Processor unit (DRE-EP). Its high level function is to receive a continuous high-rate raw data stream and to extract X-ray events data. Thanks to this on-board data processing the output data rate of the instrument is drastically reduced to be compliant with telemetry rate constraints of the mission. The DRE-EP is itself divided into two sub-assemblies: the first one is processing the data on-the-fly and is responsible for the identification of X-ray event candidates while the second sub-assembly is performing a more accurate X-ray recognition but in deferred time.

A full block diagram of the DRE-EP is depicted in Fig. 4.



Figure 4. Architecture of the DRE-EP: from left to right i) the interface with the DRE-DEMUX unit, ii) the event triggering module performing the data pre-processing, iii) the event recognition module implementing the events post-processing and the interface with the instrument control unit. This picture corresponds to 1/8 of the DRE.

#### 3.1 The event trigger

The only way to process the extremely high incoming data rate of 61.44 Gbps is to implement a highly parallelized processing. Therefore each event trigger board receives the raw data from the DRE-DEMUX by means of six serial interfaces operated at 1.28 Gbps; the whole detector array requires 8 identical boards or 48 gigabit serial links. After de-serialization the data is feeding two high performance FPGAs for real time data pixel de-multiplexing, storage in a pixel buffer and analysis. The analysis consists in identifying X-ray event candidates by applying to the pixel data stream an energy threshold as well as a timing analysis triggering criteria. When both criteria are satisfied the content of the pixel buffer that record a short pixel sampling sequence is transferred to a FIFO type buffer shared with the X-ray recognition sub-assembly.

#### 3.2 The event recognition

Unlike the event trigger sub-assembly, the event recognition sub-assembly is not processing the data on-the-fly. It successively accesses the FIFO type buffers of the event trigger function to read-back the pre-identified events. Then events are individually and accurately analyzed. When an X-ray is recognized the corresponding data are packetized and transmitted to the instrument control unit. Thanks to the modest X-ray event rate this recognition is implemented by software. A not yet defined processor executes this software; high performance processors such as LEON or PowerPC could be used either in a single or multicore version. Additional software computing requirements will help in selecting the suitable processor. In order to mitigate failure of an event recognition board a cold redundant architecture is implemented with two event recognition boards.

The event recognition software that will be implemented in the DRE-EP units for the detection and energy calculation of the events consists of three main blocks: event detection, event grading (see Ref. 8 and references therein) and energy determination (event filtering). These blocks are described hereafter.

# 3.2.1 Event detection

In this first block the input signal is filtered with a low-pass filter to reduce the noise. After that, the first derivative of the filtered signal is taken since its pronounced peak marks the steep slope of the rising pulse, and thus permits an initial detection of the events. At this stage, the small energy events on top of the biggest ones still remain hidden, requiring the subtraction of the large signal to enhance them. For this purpose the energy of the pulse is estimated with a running sum filter to select (by interpolation) the closest pulse template stored in the calibration library. This template is derived and subtracted from the first derivative of the initial signal, highlighting the smallest pulses previously masked (adjusted derivative method). At the end of this block the arrival time of the detected pulses is stored.

# 3.2.2 Event grading

The events detected in the first block enter this module to grade their quality with respect to the energy resolution. Based on the time interval between consecutive events, a grade is assigned: high-resolution (2.5 eV), mid-resolution (3.5 eV) and low-resolution (too close pulses that will have a less accurate energy estimate, around tens of eV). The energy of the low resolution events is estimated through a running sum filter while the high-resolution and mid-resolution events enter the last software block for a more accurate determination of their energy.

#### 3.2.3 Energy determination

The determination of the energy content of the high and mid-resolution events is done through the optimal filter method,<sup>9</sup> that assumes that all the pulses are scaled versions of the same signal (i.e. the detector response is linear) and that the noise is stationary. The optimal filter is created in the frequency domain as the responsivity (averaged pulse divided by its energy) divided by the square of the noise spectrum. To account for the variation of the shape of the pulses with the energy, several optimal filters (for different energies) are created during the calibration stage. Once the energy of a given event has been estimated, an interpolation is done to obtain the most accurate optimal filter to be applied to the signal. This way, the event energy can be calculated in the time domain and finally calibrated to account for the instrumental effects.

At the end of these processing blocks, the DRE-EP will provide a list with all the detected events including their arrival time, grade, energy and location on the focal plane.

# 4. ARCHITECTURE OF THE DRE

The architecture of the DRE is illustrated on Fig. 5. Its definition has been driven by the following key elements:

• To simplify the high data rate interface between these two units the DRE-DEMUX and the DRE-EP will be implemented in a same mechanical structure.

• To limit the power and the mass of a single box to "reasonable" values (with respect to the handling and power dissipation considerations) the DRE will be split in four identical units.

The last point is also an advantage with respect to the redundancy philosophy as a single failure will affect a quarter of the pixels at maximum.



Figure 5. Block diagram of one DRE unit. Such a unit processes the data of 24 readout channels (i.e. 960 pixels). Four of them are needed for X-IFU.

With this architecture we estimated the total mass of the DRE to be 168 kg and the total power consumption to be 582 W (379 W in the DRE-DEMUX and 203 W in the DRE-EP). These estimates include 20% of design maturity margins and 30% of system margins. The volume of each DRE unit will be  $350 \times 280 \times 550$  mm<sup>3</sup>.

#### 5. CONCLUSION

We described the hardware and the software parts of the Digital Readout Electronics of *Athena* X-IFU. This subsystem will be in charge of the control, readout and data processing of the front-end sensor array. it implements many critical functionalities such as: the management of the frequency multiplexing readout, the optimization of the detection chain linearity, the event detection and processing. We have defined the high level architecture of the DRE having in mind the critical requirements of the sub-system. In particular: 96 channels have to be de-multiplexed in parallel, the data of 3 840 TES based pixels have to be processed (extremely high data rate) and the DRE shall achieve a 2.5 eV energy resolution (requires an efficient onboard data processing). In the near future we will consolidate the design of the DRE and a demonstration model will be developed in the coming years.

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